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EXAMINER	
VIDWAN, JASJIT S	
ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
04/17/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Continuation of 11: Applicant argues that prior art of record fails to teach:

(a) Specifically "…the slave chip transmitting data to the host chip"

(b) No servo or related item is mentioned as it applies to the slave chip

(c) The prior art technology of removing all assistance by a processor is different than that of the present invention.

With respect to argument (a), **Examiner disagrees**. To support his argument, applicant in response filed on 03/17/08 incorrectly characterizes Examiner's interpretation of the "Slave chip" and the "Host chip" as it applies to Fujii to state that "...the transfer buffer 141 of the prior art of Fujii is interpreted by the Examiner as being equivalent to the slave unit of the present invention. Likewise, the DMA controller 121 of the prior art is interpreted to be equivalent to the host of the present invention." However, this interpretation of Examiner's position is flawed as it seems that the Applicant has only focused the prior art to include Fujii reference with no weight provided to the primary AAPA art. Examiner humbly submits that had the Examiner only used the Fujii reference as either a sole reference [35 U.S.C. 102] or as a primary reference in combinational rejection, Applicant's argument would be definitive. Unfortunately, the Office Action mailed on 12/31/07, Examiner clearly states that AAPA as a primary reference teaches a multi-chip system having a host chip and a slave chip engaged in executing servo control [see Paragraph 3, Page 3 of Final Rejection of 12/31/07]. Examiner only relies on Fujii to teach the **method** of transferring data from one location to another without the necessity of providing a duplicate established structure of a host chip and a slave chip; i.e. hypothetically Fujii's Micro-processor (element 12) and its supporting memory [(Fig 1, element 7) -- also see Col. 4, Lines 20-27] are part of AAPA's host chip, while Fujii's "Interface Unit" [Fig. 1, element 14] can either be part of or is AAPA's slave chip. The actual functionality of each unit is irrelevant as the underlying structure was established using AAPA as a primary reference.

With respect to argument (b), **Examiner disagrees**. AAPA, as was cited in Office Action mailed on 12/31/07, clearly teaches a slave chip engaged in executing servo control or signal detection [see AAPA, Paragraph 004, "…and at least a slave chip engaged in executing servo control or detecting some particular signals."]

With respect to argument (c), **Examiner disagrees**. AAPA as combined with Fujii teach having a host chip [see AAPA, Paragraph 0004, "....host chip engaged in controlling the operation of the system"] include Fujii's Microprocessor [Fig. 1, element 12]; i.e. replacing AAPA's host processor with the functionality of Fujii's microprocessor and its supporting RAM [see Fujii, Fig. 1, element 7]. Therefore, as it is clearly evident, no processing capacity has been removed from the host chip. Additionally, the above point is moot in light of the fact that claims as submitted do not include any limitation of requiring any assistance by a processor whatsoever.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASJIT S. VIDWAN whose telephone number is (571)272-7936. The examiner can normally be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JSV
4/14/08
/Alford W. Kindred/
Supervisory Patent Examiner, Art Unit 2163